

## compare.vhd

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-- Name: Roger Grayson  
-- Date: 9-10-02  
-- Purpose: Generic N-bit Comparator  
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```

```
library IEEE;  
use IEEE.std_logic_1164.all;  
use ieee.std_logic_unsigned.all;  
  
entity compare is  
    generic(N:integer:=2);  
    port( A,B: in std_logic_vector(N-1 downto 0);  
          E,L,G: out std_logic);  
end compare;  
  
architecture process_arch of compare is
```

```
begin  
    process(A,B)  
    begin  
        E <= '0'; L <= '0'; G <= '0'; --initialize  
        if A = B then E <='1'; end if;  
        if A > B then G <='1'; end if;  
        if A < B then L <='1'; end if;  
    end process;  
end process_arch;
```

```
-----  
-- Name: Roger Grayson  
-- Date: 11-5-02  
-- Purpose: 1-bit comparator  
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```

```
library IEEE;  
use IEEE.std_logic_1164.all;  
use ieee.std_logic_unsigned.all;  
  
entity compare1 is  
    port( A,B: in std_logic;  
          E,L,G: out std_logic);  
end compare1;  
  
architecture process_arch of compare1 is
```

```
begin  
    process(A,B)  
    begin  
        E <= '0'; L <= '0'; G <= '0'; --initialize  
        if A = B then E <='1'; end if;  
        if A > B then G <='1'; end if;  
        if A < B then L <='1'; end if;  
    end process;  
end process_arch;
```

