reg_file.vhd

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-- Name: Roger Grayson
-- Date: Feb 6, 2003
-- Pupr: register file
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library IEEE;
use IEEE.std_logic_1164.all;
use work.my_stuff.all;       --my package

entity reg_file is
    port (  clk,reset,WE:       in std_logic;
            WReg,SelA,SelB: in std_logic_vector(4 downto 0);
            WIN:    in std_logic_vector(31 downto 0);
            RoutA,RoutB:    out std_logic_vector(31 downto 0));
end entity reg_file;

architecture process_arch of reg_file is
signal DecOut: std_logic_vector(31 downto 0);
signal RegOut0,RegOut1,RegOut2,RegOut3,RegOut4,RegOut5,RegOut6,RegOut7,RegOut8,RegOut9,
RegOut10,RegOut11,RegOut12,RegOut13,RegOut14,RegOut15,RegOut16,RegOut17,RegOut18,RegOut19,
RegOut20,RegOut21,RegOut22,RegOut23,RegOut24,RegOut25,RegOut26,RegOut27,RegOut28,RegOut29,
RegOut30,RegOut31: std_logic_vector(31 downto 0);

begin
    decoder: dec port map (WReg,WE,DecOut);
    reg0: reg generic map (32) port map (clk,reset,DecOut(0),WIN,RegOut0);
    reg1: reg generic map (32) port map (clk,reset,DecOut(1),WIN,RegOut1);
    reg2: reg generic map (32) port map (clk,reset,DecOut(2),WIN,RegOut2);
    reg3: reg generic map (32) port map (clk,reset,DecOut(3),WIN,RegOut3);
    reg4: reg generic map (32) port map (clk,reset,DecOut(4),WIN,RegOut4);
    reg5: reg generic map (32) port map (clk,reset,DecOut(5),WIN,RegOut5);
    reg6: reg generic map (32) port map (clk,reset,DecOut(6),WIN,RegOut6);
    reg7: reg generic map (32) port map (clk,reset,DecOut(7),WIN,RegOut7);
    reg8: reg generic map (32) port map (clk,reset,DecOut(8),WIN,RegOut8);
    reg9: reg generic map (32) port map (clk,reset,DecOut(9),WIN,RegOut9);
    reg10: reg generic map (32) port map (clk,reset,DecOut(10),WIN,RegOut10);
    reg11: reg generic map (32) port map (clk,reset,DecOut(11),WIN,RegOut11);
    reg12: reg generic map (32) port map (clk,reset,DecOut(12),WIN,RegOut12);
    reg13: reg generic map (32) port map (clk,reset,DecOut(13),WIN,RegOut13);
    reg14: reg generic map (32) port map (clk,reset,DecOut(14),WIN,RegOut14);
    reg15: reg generic map (32) port map (clk,reset,DecOut(15),WIN,RegOut15);
    reg16: reg generic map (32) port map (clk,reset,DecOut(16),WIN,RegOut16);
    reg17: reg generic map (32) port map (clk,reset,DecOut(17),WIN,RegOut17);
    reg18: reg generic map (32) port map (clk,reset,DecOut(18),WIN,RegOut18);
    reg19: reg generic map (32) port map (clk,reset,DecOut(19),WIN,RegOut19);
    reg20: reg generic map (32) port map (clk,reset,DecOut(20),WIN,RegOut20);
    reg21: reg generic map (32) port map (clk,reset,DecOut(21),WIN,RegOut21);
    reg22: reg generic map (32) port map (clk,reset,DecOut(22),WIN,RegOut22);
    reg23: reg generic map (32) port map (clk,reset,DecOut(23),WIN,RegOut23);
    reg24: reg generic map (32) port map (clk,reset,DecOut(24),WIN,RegOut24);
    reg25: reg generic map (32) port map (clk,reset,DecOut(25),WIN,RegOut25);
    reg26: reg generic map (32) port map (clk,reset,DecOut(26),WIN,RegOut26);
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    reg27: reg generic map (32) port map (clk,reset,DecOut(27),WIN,RegOut27);
    reg28: reg generic map (32) port map (clk,reset,DecOut(28),WIN,RegOut28);
    reg29: reg generic map (32) port map (clk,reset,DecOut(29),WIN,RegOut29);
    reg30: reg generic map (32) port map (clk,reset,DecOut(30),WIN,RegOut30);
    reg31: reg generic map (32) port map (clk,reset,DecOut(31),WIN,RegOut31);
    muxA: mux port map (RegOut0,RegOut1,RegOut2,RegOut3,RegOut4,RegOut5,RegOut6,RegOut7,
RegOut8,RegOut9,RegOut10,RegOut11,RegOut12,RegOut13,RegOut14,RegOut15,RegOut16,RegOut17,
RegOut18,RegOut19,RegOut20,RegOut21,RegOut22,RegOut23,RegOut24,RegOut25,RegOut26,RegOut27,
RegOut28,RegOut29,RegOut30,RegOut31,SelA,RoutA);
    muxB: mux port map (RegOut0,RegOut1,RegOut2,RegOut3,RegOut4,RegOut5,RegOut6,RegOut7,
RegOut8,RegOut9,RegOut10,RegOut11,RegOut12,RegOut13,RegOut14,RegOut15,RegOut16,RegOut17,
RegOut18,RegOut19,RegOut20,RegOut21,RegOut22,RegOut23,RegOut24,RegOut25,RegOut26,RegOut27,
RegOut28,RegOut29,RegOut30,RegOut31,SelB,RoutB);

end process_arch;
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