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-- Name:     Roger Grayson
-- Date:     9-3-02
-- Purpose:  Full Adder
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library IEEE;
use IEEE.std_logic_1164.all;

entity fa is
        port(   a, b, cin:  in std_logic;
            cout, sum:          out std_logic);
end fa;

architecture structure of fa is
signal  s1, s2, s3: std_logic;   -- wires which begin and end in the component
begin
    s1 <= a and b;
    s2 <= a and cin;
    s3 <= b and cin;
    cout <= s1 or s2 or s3;
    sum <= a xor b xor cin;
end structure;
```