cpu.vhd

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----------------------------------------
-- Name: Roger Grayson
-- Date: Feb 6, 2003
-- Pupr: main CPU for Coulston computer
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library IEEE;
use IEEE.std_logic_1164.all;
use work.my_stuff.all;       --my package

entity cpu is
    port(clk, reset: in std_logic);
end cpu;

architecture behavior of cpu is
signal cw:std_logic_vector(20 downto 0);
signal sw:std_logic_vector(6 downto 0);

begin
    fsm:control port map(clk,reset,cw,sw);
    datapth:DataPath port map(cw,sw,clk,reset);
end behavior;
```