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----------------------------------------
--      Author:      Roger Grayson
--      Date: Feb, 2003
--      Purpose:a 4-bit carry look ahead adder
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library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_signed.conv_integer;
use work.my_stuff.all;       --my package

entity CLA4bit is
    port(   A,B: in std_logic_vector(3 downto 0);
            Cin: in std_logic;
            Sum: out std_logic_vector(3 downto 0);
            G,P: out std_logic_vector(3 downto 0));
end CLA4bit;

architecture behavior of CLA4bit is
signal c0,c1,c2,ovf:std_logic;
begin
    G <= A and B;
    P <= A or B;
    fa0: fa port map( a(0), b(0), Cin, c0, Sum(0));
    fa1: fa port map( a(1), b(1), c0, c1, Sum(1));
    fa2: fa port map( a(2), b(2), c1, c2, Sum(2));
    fa3: fa port map( a(3), b(3), c2, ovf, Sum(3));
end behavior;
```